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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,929	02/02/2004	In-Sung Park	5649-1230	9610

7590 09/15/2005

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EXAMINER	
LEE, CALVIN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,929	PARK ET AL.	
	Examiner	Art Unit	
	Lee Calvin	2818	

-- Th MAILING DATE of this communication app ars on th cover sheet with the corr spond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003 (Election)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/4, 12/27/4, 7/8/5*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Response to Election

1. The cancellation of claims 16-20 in the Response to Restriction, received on July 8, 2005 is acknowledged. Pending claims 1-15 are subjected for the rejections below.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 (b) that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 102(**b**) as anticipated by *Yamamoto*.

a) In re claim 1, *Yamamoto* (US 2002/0153579) teaches a method of forming a multi-layer dielectric structure, the method comprising the steps of:

-forming on semiconductor substrate **1** a first dielectric layer **3** by CVD [¶ 0073];

-forming a second dielectric layer **4** directly on the first dielectric layer [Fig. 2C], wherein the second dielectric layer **4** is formed by ALD process [¶ 0074].

b) In re claims 2 and 3, since *Yamamoto* discloses "use a composite dielectric material such as Al_2O_3 to which HFO_2, ZrO_2, La_2O_3, Y_2O_3 and the like is/are added for the amorphous dielectric film. Further, it is possible to use HfO_2, TiO_2, Ta_2O_5, BST, STO, PZT and the like for the crystalline insulating film" [¶ 0107], *Yamamoto* teaches or suggests the first and second dielectric layers comprise one selected from the group consisting of SiO_2, Si_3N_3, Ta_2O_5, HfO_2, ZrO_2, TiO_2, Y_2O_3, Pr_2O_3, La_2O_3, Nb_2O_5, $SrTiO_3$ (STO), $BaSrTiO_3$ (BST) and $PbZrTiO_3$ (PZT).

c) In re claim 6, *Yamamoto* discloses forming first dielectric layer **3** by ALD also [¶ 0072], and forming second dielectric layer **4** by CVD instead [¶ 0075].

d) In re claims 7-8, *Yamamoto* teaches or suggests the first and second dielectric layers comprise one selected from the group consisting of $Si0_2$, Si_3N_3, Ta_20_5, $Hf0_2$, $Zr0_2$, $Ti0_2$, Y_20_3, Pr_20_3, La_20_3, Nb_20_5, $SrTi0_3$ (STO), $BaSrTi0_3$ (BST) and $PbZrTi0_3$ (PZT) [¶ 0107].

Claim Rejections - 35 U.S.C. § 102 or § 103

4. Claims 10, 14, and 15 are rejected under 35 U.S.C. 102(**b**) as anticipated by or, in the alternative, under 35 U.S.C. 103(**a**) as obvious over *Won et al* (US 2004/0141390).

a) In re claim 10, *Yamamoto* also teaches a method of forming a capacitor, comprising of:

-forming a first electrode **9** on a substrate

-forming on the first electrode a first dielectric layer **3** by ALD [Fig. 7C and ¶ 0102];

-forming second and third dielectric layers on the first dielectric layer by ALD or CVD [¶ 0103];

-and forming a second electrode **10** on the third dielectric layer **6** [¶ 0104]

In the first embodiment [Fig. 2D & 3], *Yamamoto* teaches a MOSFET having an electrode formed on a two-layer dielectric structure; wherein the first dielectric layer **3** can be formed by ALD [¶ 0085] or by CVD [¶ 0086], and the second dielectric layer **4** can be formed by ALD or by CVD [¶ 0088]. In this third embodiment, *Yamamoto* teaches a DRAM having a three-layer dielectric structure instead of a two-layer dielectric structure. *Won et al* discloses a semiconductor capacitor of a DRAM having "a dielectric layer is one of an AlO/TaO, an AlO/TaO/AlO layer, a TaO layer, an AlO layer, an AlO/HfO layer, and a HfO layer" [¶ 0040].

It would have been an obvious matter of design choice to have a capacitor with a two-layer dielectric structure instead of a three-layer dielectric structure, since such a modification would have involved a mere change in the size of the dielectric structure. Moreover, the Examiner notes that, in *Park et al* [¶ 0041], "dielectric layer **130** formed of a multiple layer such as the AlO/TaO layer, the AlO/HfO layer, and the ATA layer rather than a single layer ... show *superior electrical* properties in respect to the breakdown voltage of 10nA under the same Toxeq."

b) In re claims 14-15, since *Yamamoto* discloses "use a composite dielectric material such as Al_2O_3 to which HfO_2, ZrO_2, La_2O_3, Y_2O_3 and the like is/are added for the amorphous dielectric film. Further, it is possible to use HfO_2, TiO_2, Ta_2O_5, BST, STO, PZT and the like for the crystalline insulating film" [¶ 0107], *Yamamoto* teaches or suggests the first and second dielectric layers comprise one selected from the group consisting of SiO_2, Si_3N_3, Ta_2O_5, HfO_2, ZrO_2, TiO_2, Y_2O_3, Pr_2O_3, La_2O_3, Nb_2O_5, $SrTiO_3$ (STO), $BaSrTiO_3$ (BST) and $PbZrTiO_3$ (PZT).

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 9 are rejected under 35 U.S.C. 103(**a**) as being unpatentable over *Yamamoto* as applied to claims 1 and 6, in view of *Hegde et al* (US 2003/0176049).

Yamamoto suggests "the two layer structure comprising a first dielectric film which is made of amorphous oxide such as Al_2O_3 and the like and a second dielectric film which is made of metal oxide such as ZrO_2, HfO_2, and the like." *Yamamoto*, however, does not explicitly suggest the first dielectric layer includes $Hf0_2$ and the second dielectric layer includes Al_20_3. *Hegde* et al discloses a bottom dielectric **26** of HfO_2 and a top dielectric **24** Al_2O_3 [¶ 0015].

It would have been obvious to one having skills in the art to have modified the dielectric formation of *Yamamoto* by utilizing Al_2O_3 material as the top dielectric layer for the purpose of "minimizing the thickness of the Al_2O_3 in order to make the dielectric constant of the gate dielectric **14** as high as possible" [¶ 0015].

7. Claim 5 is rejected under 35 U.S.C. 103(**a**) as being unpatentable over *Yamamoto* as applied to claim 1, in view of *Park et al* (US 2003/0235947).

Although *Yamamoto* is silent about pressure in the layer formation, *Yamamoto* at least suggests forming first dielectric layer **3** at a temperature of 300°C [¶ 0085], and second dielectric layer **4** at a temperature of 300°C [¶ 0087]. *Park et al* teaches forming high-k dielectric layers by ALD, "a third dielectric thin layer **28** is formed by depositing a Ta_2O_5 layer on the second dielectric thin layer **27** ... a temperature and a pressure are maintained within a range from about 200°C to about 500°C and from about 0.1Torr to about 1.0Torr" [¶ 0036].

It would have been obvious to one having skills in the art to have modified the dielectric formation of *Yamamoto* by utilizing pressure(s), suggested by *Park et al*, for the purpose of supporting one of the advantages of ALD process in layer formation --the control of a layer thickness on an atomic layer level-- by utilizing a relatively lower pressure, which is related to a low temperature (compared to the temperature applied to form a layer by CVD, for instance).

8. Claims 11-13 are rejected under 35 U.S.C. 103(**a**) as being unpatentable over *Yamamoto* (or, in the alternative, in view of *Won et al*), further in view of *Jeong et al* (US 2004/0106252)

a) In re claim 11, although *Yamamoto* discloses "providing different chamber portions ... for performing a film forming process" [¶ 0113] in the apparatus [Fig. 8], *Yamamoto* does not explicitly disclose forming the first and second dielectric layers in first and second chambers, respectively. *Jeong et al* suggests [¶ 0066] forming a first dielectric layer in a first chamber **411** [step **S20** of Fig. 5], and a second dielectric layer in a second chamber **414** [step **S40** of Fig. 5].

It would have been obvious to one having skills in the art to have modified the film forming process of *Yamamoto* by specifying first chamber for the first layer and second chamber for the second layer for the purpose of "perform different process continuously without waiting until the temperature for each process settles to a desired value and within the same vacuum condition" [mentioned by *Yamamoto* in paragraph 0113].

b) In re claims 12-13, *Yamamoto* discloses transferring the substrate after forming the first dielectric layer in a chamber **12** while maintaining a vacuum on the substrate (being transferred within the three-chamber apparatus) via a transfer chamber **13** configured to be selectively coupled to a film forming chamber **12** [Fig. 8]. Moreover, *Jeong et al* describes an apparatus having a transfer chamber **409** coupled between first and second chamber **411** and **414** [Fig. 13].

It would have been obvious to one having skills in the art to have modified the film forming apparatus of *Yamamoto* by utilizing a transfer chamber selectively coupled to first and second chambers for the purpose of efficiently forming multilayer dielectric structure without waiting for preheating (or cooling off) the film forming chambers.

Contact Information

9. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30 (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The central fax number for the organization (where this application is assigned to) is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http:/pair-direct.uspto.gov. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.

Calvin Lee

Dated: September 13, 2005